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## Hardware Implementation for Motion Estimation in Real Time Scenario

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### Abstract

Motion estimation (ME) is a multistep process that involves not one, but a combination of techniques, such as motion starting point, motion search patterns, and adaptive control to limit the search, avoidance of search stationary regions, etc. The collective efficiency of these techniques is what makes a ME algorithm robust and efficient. This paper proposes a ME algorithm that is an embodiment of several effective ideas for finding the most accurate motion vectors (MVs) with the aim to maximize the encoding speed as well as the visual quality.

Here we developed a hardware approach in which a frame of pictures are captured and sent via serial port to the system. With the help of MATLAB we are going to find out whether any motion is there in the frames. Once any motion is been estimated that signal is sent to the hardware it will give us appropriate sign accordingly. This system is developed on two platforms (hardware as well software).

Keywords: Bit plane matching algorithm, Gray coding, Variable block size motion estimation, Hardware Architecture.

## Introduction

Variable Block Size Motion Estimation (VBSME) is one of the essential features of state-of-the-art video coding standards, such as H.264/AVC [1], by which better motion compensation can be performed as a result of higher coding accuracy achieved by using smaller blocks and the flexibility in the combination of variable size blocks. However, the computational complexity of such an ME scheme as utilized in the H.264/AVC encoder is extremely high for real time operation. Thus, efficient methods for implementing high performance and low computational complexity video coding methods and hardware architecture design with low- power and high data throughput are essential for new consumer electronics products, and in particular mobile Devices.

About 75% of the computational load of the H.264/AVC encoder is occupied by integer motion estimation (IME) [2]. For integer motion estimation process, the current video Frame is divided into none overlapping macro blocks (MB) typically of size  $16 \times 16$  pixels. For VBSME, the current MB is further divided into smaller sub blocks of size  $8 \times 8$  pixels For example. In H.264, there are 7 different sub block

types of sizes  $16\times16$ ,  $8\times16$ ,  $16\times8$ ,  $8\times8$ ,  $4\times8$ ,  $8\times4$  and  $4\times4$  pixels.

A hardware architecture that is to support such an ME scheme should generate and evaluate all motion vectors (MV) of these sub blocks. The most efficient way of performing VBSME is to compute the matching of all 4×4 sub blocks within an MB and then merge the results to obtain the matching of larger blocks of different size. Most of the previously proposed approaches presented in the literature have adopted the sum of absolute differences (SAD) as a matching criterion for N × N pixel sized block, as provided in (1) where c(), r(), (m,n) and, s denote current block pixel, candidate block pixel, candidate displacement, and search range respectively [3]-[4].

$$SAD(m,n) = \sum_{i=0}^{N-1} \sum_{j=0}^{N-1} |c(i,j) - r(i+m,j+n)|$$
  
-s \le m, n \le s  
$$MV = \min(SAD(m,n))$$
 (1)

An alternative matching criterion which is proposed to reduce the computation complexity of the ME

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operation is the bit plane matching (BPM) technique. In BPM based methods, instead of the sum of absolute differences, logical exclusive or (EXOR) operations are adopted for block matching. Thus, computational complexity is reduced at the cost of a loss in ME accuracy.

$$NNMP(m,n) = \sum_{i=0}^{N-1} \sum_{j=0}^{N-1} B^{i}(i,j) \oplus B^{i-1}(i+m,j+n)$$
  
-s \le m,n \le s (2)

 $MV = \min(NNMP(m, n))$ 

The Number of Non-Matching Points (NNMP) that is given in (2) is typically used in BMP for matching, where logical EXOR operation and MV shows the motion vector of the corresponding block. Bt (i, j) and Bt -1 (i, j) represent the pixels in the bit planes on Time t and t -1 respectively. The bit plane (BP) of the related video frame, which is represented as B (i, j) can be derived as

$$B(i,j) = \begin{cases} 1, \text{ if } I(i,j) \ge I_F(i,j) \\ 0, \text{ otherwise} \end{cases}$$
(3)

Where, I and F I represent the original and filtered versions of the related video frame respectively. Although the NNMP operation shown in (2) is quite simple, the filtering operation required to obtain the BPs is a new problem, from the hardware architecture point of view.

### Hardware components

### A. Microcontroller

The AT89C52 is a low-power, high-performance CMOS 8-bit microcomputer with 8K bytes of Flash programmable and erasable read only memory (PEROM). The device is manufactured using Atmel's high-density nonvolatile memory technology and is compatible with the industry-standard 80C51 and 80C52 instruction set and pin out. The on-chip Flash allows the program memory to be reprogrammed insystem or by a conventional nonvolatile memory programmer. By combining a versatile 8-bit CPU with Flash on a monolithic chip, the Atmel AT89C52 is a powerful microcomputer which provides a highly-flexible and cost-effective solution to many embedded control

The AT89C52 provides the following standard features: 8K bytes of Flash, 256 bytes of RAM, 32 I/O lines, three 16-bit timer/counters, a six-vector two-level interrupt architecture, a full-duplex serial port, on-chip oscillator, and clock circuitry. 64 Kbytes of external program memory space, 64

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Kbytes of external data memory space In addition, the AT89C52 is designed with static logic for operation down to zero frequency and supports two software selectable power saving modes. The Idle Mode stops the CPU while allowing the RAM; timer/counters, Serial port, and interrupt system to continue functioning. The Power-down mode saves the RAM contents but freezes the oscillator, disabling all other chip functions until the next hardware reset.

The At89c52 microcontroller is described in detail in the At89c52 Datasheet that can be found on official Atmel website.

#### **B.IR Sensor**

An infrared sensor is an electronic device that emits and/or detects infrared radiation in order to sense some aspect of its surroundings. Infrared sensors can measure the heat of an object, as well as detect motion. Many of these types of sensors only measure infrared radiation, rather than emitting it, and thus are known as Passive infrared (PIR) sensors.

## C. Optocoupler-PC817

There are many situations where signals and data need to be transferred from one subsystem to another within a piece of electronics equipment, or from one piece of equipment to another, without making a direct ohmic electrical connection. Often this is because the source and destination are (or may be at times) at very different voltage levels, like a microprocessor which is operating from 5V DC but being used to control a triac which is switching 240V AC.

In such situations the link between the two must be an isolated one, to protect the microcontroller from overvoltage damage.

PC817X Series contains an IRED optically coupled into a phototransistor. It is packaged in a 4pin DIP, available in wide-lead spacing option and SMT gull wing lead-form option.

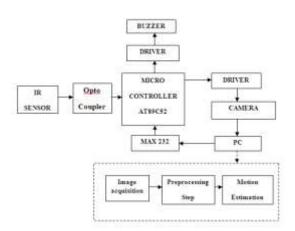
Input-output isolation voltage (rms) is 5.0kV, current of 5mA. 4pin DIP package. It is having applications as

- 1. I/O isolation for MCUs (Micro Controller Units)
- 2. Noise suppression in switching circuits
- 3. Signal transmission between circuits of different potentials and impedances

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# fig 1:Block diagram representation of working principle

Block comprises of AT89C52 micro controller, IR sensor, Opto coupler-pc817, Drivers, camera, buzzer, MAX232, PC

IR sensors are placed where the motion of the object has to be detected. When any obstacle present between the sensors then controller makes the camera on automatically. Camera will take the pictures of the object with some time delay. In Pc after image acquisition and with the help of mat lab programming some pre processing steps will be done for the images like resizing, converting RGB image in to gray. These pre processing steps are needed to reduce the computational time. Bit plane matching algorithm is used to estimate the motion of the object. The motion of a person is output to the hardware resulting in sounding the buzzer.

## **Experimental results**

To test the motion of the object, images are taken with the help of camera. Images were simulated using Mat lab 7 version.



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## **Block diagram**



Fig 2 Input Images

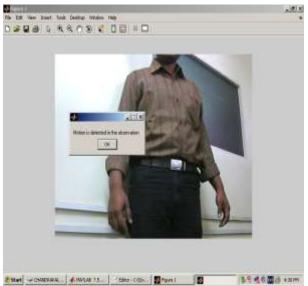


Fig 3: The above input images are converted in video format and motion is estimated by using Bit plane matching algorithm

## Applications

Basically the method which is proposed will give an intimation about a person and its behavior at the working (where the design is placed) environment. So that the person at the control unit will be having an idea about the particular individuals characteristics by the motion of his body.

- 1. Suppose if a person in ATM should move towards the machine. If he moves towards server and does some damage the control unit must be able to detect the particular person. In this scenario if we detect the motion of that person we can easily tell the particular person has made some damage to the machine or server.
- 2. In any authenticated places we can use this hardware according to the environment requirements where motion plays a great role.
- 3. For blind people, if this hardware is kept inside their stick he can analyze the obstacle

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easily whether its movement is towards him or away from him.

## **Future work**

As the Internet is more and more universal and the technology of multimedia has been progressed, the communication of the image data is a part in life. In order to employ effect in a limit transmission bandwidth, to convey the most, high quality user information .It is necessary to have more advanced compression method in image and data. Motion Estimation (ME) and compensation techniques, which can eliminate temporal redundancy between adjacent frames effectively, have been widely applied to popular video compression coding standards such as MPEG- 2, MPEG-4. Full search Motion Estimation algorithm is not fit for real-time applications because of its unacceptable computational cost. Bidirectional ME forms a major computation bottleneck in video processing applications such as the detection of noise in image sequences, interpolation/ prediction of missing data in image sequences and de interlacing of image sequences

### References

- 1. Joint Video Team (JVT) of ISO/IEC MPEG & ITU-T VCEG, "Draft ITU-T Recommendation and Final Draft International Standard of Joint Video Specification (ITU-T Rec. H.264/ISO/IEC 14496-10 AVC)", JVT-G050, March, 2003.
- C.Y. Chen, W.Y. Chien, Y.W. Huang, T.C. Chen, T.C. Wang, L.G. Chen, "Analysis and Architecture Design of Variable Block-Size Motion Estimation for H.264/AVC", IEEE Tran. Circuits Syst. vol. 53, no. 2, pp.578-593, Mar. 2006.
- T.-C. Chen, Y.-H. Chen, S.-F. Tsai, S.-Y. Chien, L.-G. Chen, "Fast Algorithm and Architecture Design of Low-Power Integer Motion Estimation for H.264/AVC", IEEE Trans. Circuits and Syst. Video Technol., vol. 17, no. 5, pp. 568-577, May 2007.
- C. Wei, H. Hui, T. Jiarong, and M. Hao, "A High-performance Reconfigurable VLSI Architecture for VBSME in H.264", IEEE Trans. on Consumer Electron., vol. 54, no. 3, pp. 1338-1345, Aug. 2008.B. Natarajan, V. Bhaskaran, and K. Konstantinides, "Lowcomplexity block-based motion estimation via one-bit transforms", IEEE Trans. Circuit Syst. Video Technol., vol. 7, no. 4, pp. 702-706, Aug. 1997.

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